operation;

a second plurality of electronic components defining a non-instant on mode of operation;

a plurality of input/output devices; and

one or more switching mechanisms to selectively couple one or more of said plurality of input/output devices to one or more of said first plurality of electronic components and enable said apparatus to start up in said instant on mode of operation to the exclusion of said second plurality of electronic components, or to selectively couple said one or more input/output devices to one or more of said second plurality of electronic components and enable said apparatus to start up in said non-instant on mode of operation to the exclusion of said first plurality of electronic components.

3. (Amended) The apparatus of claim 2, wherein said first plurality of electronic components includes a first memory device and said second plurality of electronic components includes a second memory device, and wherein after start up said first and second processors operate simultaneously to synchronize data between said first and second memory devices.

4. (Amended) The apparatus of claim 1, wherein at least one of said first and second plurality of electronic components includes a processor having at least two operating modes, wherein when in a first operating mode said processor executes instructions representing a first operating system, and when in a

second operating mode said processor executes instructions representing a second operating system.

8. (Amended) An apparatus comprising:

an integrated circuit having a plurality of function blocks for use in a first instant on mode of operation;

a plurality of electronic components for use in a second non-instant on mode of operation;

a plurality of input and output devices; and

one or more switching mechanisms to selectively couple one or more of said plurality of input and output devices to one or more of said function blocks to enable said one or more input and output devices to be available for use in said first instant on mode of operation to the exclusion of said a plurality of electronic components, or to selectively couple said one or more of said plurality of input and output devices to one or more of said plurality of electronic components to enable said one or more input and output devices to be available for use in said second non-instant on mode of operation to the exclusion of said plurality of function blocks.

11. (Amended) The apparatus of claim 9, wherein said plurality of function blocks includes a first memory device, wherein said second plurality of electronic components includes a second memory device, and wherein after start up said first and second processors operate simultaneously to synchronize data stored

within said first and second memory devices.

12. (Amended) The apparatus of claim 8, wherein at least one of said plurality of function blocks and said plurality of electronic components include a processor having at least two operating modes, wherein when in a first operating mode, said processor executes instructions representing a first operating system, and when in a second operating mode, said processor executes instructions representing a second operating system.

16. (Amended) An integrated circuit comprising:

a first processor block to operate in a first instant on mode of operation;

a second processor block to operate in a second non-instant on mode of operation;

a plurality of input/output ports; and

one or more switching mechanisms to selectively couple one or more external devices to said first processor block through at least one of said plurality of input/output ports to facilitate use of said one or more external devices in said instant on mode of operation to the exclusion of said second processor block, or to selectively couple said one or more external devices to said second processor block through at least one of said plurality of input/output ports to facilitate use of said one or more external devices in said non instant on mode of operation to the exclusion of said first processor block.

18. (Amended) The integrated circuit of claim 16, wherein said plurality of external devices includes a first memory device and a second memory device, and wherein after start up said first and second processor blocks operate simultaneously to synchronize data between said first and second memory devices.

21. Cancelled without prejudice.